IN THE CLAIMS

Please amend the claims as follows:

1. (original) A method of compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the method being characterized by the steps of:
(i) comparing corresponding bits of two or more subsequent vectors to determine if they are compatible; and, if all corresponding bits of said vectors are compatible;
ii) merging said two or more vectors to create a single vector representative thereof; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values.

2. (original) A method according to claim 1, wherein said data comprises test vector data for use in testing a logic product, and the method includes the steps of generating or obtaining original test vector data comprising "care" bits and "don't care "bits", and compressing said test vector data according to steps i) and ii).

3. (original) A method according to claim 2, wherein said original test vector data is generated by means of an Automated Test Pattern Generation (ATPG) tool.

4. (currently amended) A method according to ~~any one of claims 1 to 3~~claim 1, including the step of generating a repeat value in respect of one or more merged vectors, said repeat value being indicative of a number of times the respective merged vector should be repeated to reconstruct the care bits in the vectors of which the merged vector is representative.

5. (original) A data set comprising test vector data for use in testing a logic product, said test vector data being compressed by the method of claim 4.

6. (original) A method of testing a logic product, the method comprising the steps of generating compressed test vector data according to claim 5, reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the resultant output data.

7. (currently amended) A method according to claim 6, further comprising the step of compressing said output data ~~according to any one of claims 1 to 4~~ comprising a sequence of at least two

subsequent vectors, wherein a vector comprises one or more bits, the method being characterized by the steps of:

(i) comparing corresponding bits of two or more subsequent vectors to determine if they are compatible; and, if all corresponding bits of said vectors are compatible;

ii) merging said two or more vectors to create a single vector representative thereof; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values.

8. (original) Apparatus for compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by:

i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are compatible; and

ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values.

9. (original) Apparatus according to claim 8, wherein said data comprises test vector data for use in testing a logic product, and

the apparatus includes means for generating or receiving original test vector data comprising a sequence of two or more vectors, wherein a vector comprises one or more bits, including "care" bits and "don't care" bits.

10. (original) Apparatus for testing a logic product, including means for generating original test vector data, apparatus for compressing said original test vector data according to claim 9, means for reconstructing said test data from said compressed data, means for applying said reconstructed data to an input of said logic product, and means for obtaining the resultant output data.

11. (original) Apparatus according to claim 10, wherein said don't care bits are randomly filled in the case of test vector data comprising a sequence of <n vectors, while said don't care bits are filled by merging compatible vectors in the case of test vector data comprising a sequence of ≥n compatible vectors.

12. (currently amended) Apparatus according to claim 10, including apparatus ~~according to claim 8~~ for compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by:

i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are compatible; and

ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values for compressing said output data.

13. (currently amended) Apparatus according to ~~any one of claims 10 to 12~~claim 10, wherein said means for generating original test vector data comprises an Automated Test Pattern Generation (ATPG) tool.

14. (original) Apparatus according to claim 13, including means for reordering a test pattern, prior to compression thereof.

15. (original) Apparatus according to claim 10, including means for storing merged data sequences in the form of a data set for use in testing a logic product.

16. (original) Electronic data storage means on which is stored a data set created by means of apparatus according to claim 15.